10-27-00

Express Mail Number: EL052830140US Docket No. B-3650 617089-5

Date: October 25, 2000

JC853 U.S. PTO 10/25/00

JC929 U.S. PTO 09/696826 10/25/00

Commissioner of Patents and Trademarks
Box New Patent Application
Washington, D.C. 20231

Sir:

NEW APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of

Inventor(s): (1) William M. Clark, Jr. (2) James P. Baukus
(3) Lap-Wai Chow

NOTE: Patent must be applied for in the name of all of the actual inventor or inventors.

For: "IMPLANTED HIDDEN INTERCONNECTIONS IN A SEMICONDUCTOR DEVICE FOR PREVENTING REVERSE ENGINEERING"

Enclosed are:

1. **The Papers Required For Filing Date Under 37 CFR 1.53(b):**

9 Pages of specification 1 Page of abstract 3 Pages of claims

2 Sheets of drawings [X] formal [ ] informal
(Figs. 1-5)

[X] In addition to the above papers there is also attached
1 Page of a Preliminary Amendment dated October 25, 2000.

Postcard
Check for filing fee in the amount of $710.00
Declaration/Power of Attorney (4 pages)
Assignment Cover Sheet (1 page), Assignment document (2 pages), and Check for $40.00

CERTIFICATION UNDER 37 CFR 1.106

I hereby certify that this paper and the documents referred to as enclosed therein are being deposited with the United States Postal Service in an Express Mail envelope with sufficient postage for Express Mailing on this date October 25, 2000 in an envelope as "Express Mail Post Office to Addressee" Mailing Label Number EL052830140US addressed to the:

Commissioner of Patents and Trademarks
Box New Patent Application
Washington, D.C. 20231

Karyn Lao
(Typed or printed name of person mailing paper)

(Signature of person mailing paper)

NOTE: Each paper or fee referred to as enclosed herein has the number of the "Express Mail" mailing label placed thereon prior to mailing. 37 CFR 1.10(b).

2. Declaration or oath

[X] Enclosed

[X] original [ ] facsimile

executed by:

[X] inventor(s)

[ ] legal representative of inventor(s) 37 CFR 1.42 or 1.43

[ ] joint inventor or person showing a proprietary interest on behalf of inventor who refused to sign or cannot be reached. 37 CFR 1.47.

[ ] petition and statement required by 37 CFR 1.47 also attached. See item 7 below for fee.

[ ] Not Enclosed

[ ] Application is made by a person authorized under 37 CFR 1.41(c) on behalf of all of the above named inventor(s). The declaration or oath, along with the surcharge required by 37 CFR 1.16(e) can be filed subsequently.

[ ] Showing that the filing is authorized. (Not required unless called into question. 37 CFR 1.41(d)).

NOTE: Where the filing is a completion in the U.S. of an international application under 35 U.S.C. 371(c)(4) then the declaration must be filed.

3. Assignment

[X] An assignment of the invention to HRL Laboratories, LLC (with separate cover sheet and separate check for $40.00)

4. Certified Copy

[ ] A certified copy of Application from which priority is claimed.

NOTE: Must be referred to in oath or declaration. 37 CFR 1.55 and 163.

5. Fee Calculation

CLAIMS AS FILED			
Number Filed	**Number Extra**	**Rate**	**Basic Fee $ 710.00**
Total Claims 14 -20=	0 x	$ 18.00	0
Independent Claims 3 -3=	0 x	$ 80.00	0
Multiple Dependent Claim(s), If Any	0 x	$270.00	0

[ ] Amendment canceling extra claims enclosed

[ ] Amendment deleting multiple dependencies enclosed

[ ] Fee for extra claims is not being paid at this time

NOTE: If the fee for extra claims are not paid on filing they must be paid or the claims canceled by amendment, prior to the expiration of the time period set for response by the Patent and Trademark Office in any notice of fee deficiency, 37 CFR 1.16(d).

Filing Fee Calculation $ 710.00

6. Small Entity Statement

[ ] Verified statement that this is a filing by a small entity under 37 CFR 1.9 and 1.27.

Filing Fee Calculation (50% of above) $_____

NOTE: If a verified statement is filed within 2 months of the date of payment of first fee then the excess fee paid will be refunded on request. Notice of January 20, 1983. 1027 TMOG 114.

7. Fee Payment Being Made At This Time

[ ] Not Enclosed

[ ] No filing fee is submitted. This and the surcharge required by 37 CFR 1.16(e) can be paid subsequently.

NOTE: Where the filing is a completion in the U.S. of an international application the fee must be paid.

[X] Enclosed

[X] filing fee $ 710.00

[ ] recording assignment ($40.00; 37 CFR 1.21(h)(i)) $_____

[ ] petition fee for filing by other than all the inventors or person on behalf of the inventor where inventor refused to sign or cannot be reached. 37 CFR 1.47 and 1.17 (h) $_____

Total fees enclosed $ 710.00

8. Method of Payment of Fees

[X] check in the amount of $ 710.00

[ ] charge account No. 12-0415 in the amount of $_____
A duplicate of this transmittal is attached.

NOTE: Fees should be itemized is such a manner that it is clear for which purpose the fees are paid. 37 CFR 1.22(b).

9. Authorization to Charge Additional fees

[X] The Commissioner is hereby authorized to charge the following additional fees which may be required to Account No. 12-0415:

[X] 37 CFR 1.16 (filing fees and presentation of extra claims)

[X] 37 CFR 1.17 (application processing fees)

[ ] 37 CFR 1.18 (issue fee at or before Mailing of Notice of Allowance, pursuant to 37 CFR 1.311(b))

NOTE: 37 CFR 1.28(b) requires "Notification of any change in loss of entitlement to small entity status must be filed in the application...prior to paying... issue fee".

10. Instructions As To Overpayment

[X] Credit Account No. 12-0415 [ ] refund

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EL052830140US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: William M. Clark, Jr. et al.
Serial No.: Not yet assigned
Filed: Concurrently herewith
For: "IMPLANTED HIDDEN INTERCONNECTIONS IN A SEMICONDUCTOR DEVICE FOR PREVENTING REVERSE ENGINEERING"

Re: Preliminary Amendment

Our Ref: B-3650 617089-5

Date: October 25, 2000

Commissioner of Patents and Trademarks
Box New Patent Application
Washington, D.C., 20231

Sir:

Prior to examination of the above-identified application, it is respectfully requested that the following amendments be made to the Specification and Declaration/Power of Attorney:

IN THE SPECIFICATION

Page 7, Line 12 Please change "interconnection" to --interconnections--.

Please change the Residence and Post Office Address of James P. Baukus to read as follows:

1137 Paquita Street, Westlake Village, California 91361

REMARKS

Amendment of the subject application is respectfully requested.

Respectfully submitted,

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Implanted Hidden Interconnections in a Semiconductor Device for Preventing Reverse Engineering

Technical Field

The present invention relates to semiconductor devices and their methods of manufacture wherein the semiconductor devices have implanted interconnections which are hidden and/or camouflaged so as to inhibit or prevent reverse engineering of the semiconductor device.

Background of the Invention

The design and development of semiconductor Integrated Circuits (ICs) tends to be rather expensive and, in fact, many hours of engineering talent are required to develop the complex structures, processes and manufacturing techniques involved in making modern semiconductor devices and ICs. Indeed, semiconductor ICs over the years have tended to become more complex and therefore the effort involved in achieving a successful design has become very expensive. Many man-hours of highly skilled professional time are required at considerable expense to design and develop a modern integrated circuit.

Others, in order to avoid not only the expense involved in the design and development of integrated circuits, but also to avoid the significant time involved in bringing a new integrated circuit design to the market place, resort to reverse engineering practices for existing integrated circuits to take apart, probe, and otherwise examine these existing ICs to try to determine the physical structures and methods used to make the integrated circuit for subsequent copying. This

reverse engineering, which typically relies primarily on obtaining planar optical images of a circuit, in essence tries to bypass the typical product development cycles and expenses involved in producing integrated circuits.

Since the reverse engineer is trying to go for a "free ride" on the efforts of others, various approaches have been developed to try to thwart the reverse engineer, particularly in the field of semiconductor integrated circuits. See, for example, U.S. Patent No. 4,583,011 wherein the device is given a depletion implant that is virtually invisible to a reverse engineer.

Integrated circuits typically comprise a large number of active devices, typically in the form of transistors, diodes, and the like, which are interconnected by the means of interconnects. The interconnects are often provided by metallic structures which are formed on various levels within an integrated circuit device. Since these metallic structures etch away in the presence of an appropriate etchant at a different rate compared to the other structures found in a semiconductor device (such as semiconducting material, insulating material, and the like), the reverse engineer can discover the presence and the structure of metallic conductors used to interconnect the active devices in an integrated circuit by putting the needed time and energy into the reverse engineering task. However, since this time and energy is less than that required to design a new IC, reverse engineering has its followers. Indeed, the reverse engineer's object is to make a working, slavish copy of the original IC and the reverse engineer cares little about how the original IC was designed. The reverse engineer does not seem to be deterred by the fact that in many countries existing ICs are legally protected against copying by some form of mask works protection. As such, in order to protect the considerable investment made in new IC designs, other or additional steps are needed to deter such slavish copying.

Summary of the Invention

The present invention provides a method and apparatus for preventing reverse engineering of integrated circuits by hiding interconnects between various devices and structures (for example, diodes, transistors, input/output connections, power supply connections and the

like) so as to make it much more difficult for the reverse engineer to determine how the devices and structures, which can be seen on an integrated circuit, are interconnected.

In one aspect, the present invention provides an interconnect for interconnecting two spaced-apart implanted regions of a common conductivity type in an integrated circuit or device. The interconnect comprises a first implanted region forming a conducting channel between the two spaced-apart implanted regions, the conducting channel being of the same common conductivity type and bridging a region between the two spaced-apart regions, and a second implanted region of opposite conductivity type, the second implanted region being disposed between the two spaced-apart implanted regions of common conductivity type and being disposed over the conducting channel.

In another aspect the present invention provides a method of providing and camouflaging an interconnect between two adjacent implanted regions in an integrated circuit or device, the two adjacent implanted regions being of a common conductivity type. The method includes implanting a first region of the same common conductivity type, the first region being disposed between locations where said two adjacent implanted regions either have been or will be formed; and implanting a second region of opposite conductivity type to the common conductivity type, the second region over-lying the first region and having a concentration profile normal to a major surface of the integrated circuit or device with a concentration peak closer to the major surface of the semiconductor device than a concentration peak for the first implanted region.

Brief Description of the Drawings

Figure 1 shows a side sectional view through a semiconductor device or IC showing a portion of two active devices with a hidden implant providing an interconnect there between;

Figure 2 is similar to Figure 1, but the priority types of the devices and the interconnect have been reversed, compared to Figure 1;

Figure 3 is similar to Figure 1, but no interconnect is provided between the active areas of

the two transistors;

Figure 4 is similar to Figure 3, but the camouflaging implant shown in Figure 3 has been omitted;

Figure 5 is a plan view of a semiconductor device or IC having a number of implanted regions forming active regions of active devices therein, some of which are interconnected in accordance with the present invention.

Detailed Description

Figure 1 is a cross sectional view through a portion of a two interconnected active devices 1, 2 in an integrated circuit. Only a portion of two active devices are shown in Figure 1 since this invention is concerned with techniques for camouflaging the interconnections rather than with the structure of the devices *per se*. The portion of active device 1 which is depicted is a N-type region 11 which could provide the drain, for example, of a first FET transistor 1 and could be formed as an implanted region with a N-type dopant by techniques very well known in the art. Those skilled in the art will recognize, of course, that the N-type region 11 could alternatively form a portion of a diode, a portion of a bipolar transistor or a portion of some other semiconductor structure. The portion of active device 2 which is depicted is a N-type region 12 which could form the source, for example, of a second FET transistor 2.The function or functions attributed to regions 11 and 12 are not particularly important to the present invention and they could represent any implanted semiconductor structure as a matter of design choice.

A complicated integrated circuit can literally comprise millions of active regions. Of course, not all active regions or devices are connected to an immediately adjacent active region or device although that is not infrequently the case. With respect to Figure 1, it is assumed that active region 11 and active region 12 require, due to the design of the integrated circuit device in which they are used, interconnection. In the prior art, they might well have been interconnected by providing a thin layer of gold, aluminum or other metallic conductor on the presently exposed surface 15 between implanted regions 11 and 12. However, according to the present invention,

regions 11 and 12 are interconnected by a N-type implanted region 13 which provides a conduction channel that interconnects the two active regions 11, 12. In order to camouflage the N-type implant 13, an implant of opposite conductivity type, for example, P-type conductivity type here, is implanted in a shallower region 14 immediately above the conductive channel formed by region 13.

Those skilled in the art will realize that if the P-type implant 14 were not employed, that the N-type implant 13, which would tend extend towards the surface 15 of the semiconductor device shown in Figure 1, might be discoverable by stain and etch techniques. Depending on the type of implantation used, the concentration of the N-type dopant could well be higher in regions below surface 15 compared to regions immediately adjacent surface 15. The relatively deeper N-type implant 13 provides a conduction path and will most likely have a relatively high dose of dopant to form the implant (for example, the amount of dosage of the dopant in the conduction path implant 13 could be the same as the dosage used to implant the active regions 11 and 12). The camouflaging implant, namely, implant 14 is also a relatively heavy implant, in order to camouflage the opposite conductivity type material in region 13 forming the conducting channel. However, the camouflaging implant 14 is relatively shallow compared to the depth of the conducting implant 13.

Preferably the depth of the camouflaging implant 14 will be on the order of 0.1μm while the depth of the conducting channel implant 13 will be on the order of 0.2 μm for FET transistor structures of the type partially depicted in Figure 1. In the case of FET transistor structures, those skilled in the art will appreciate that active regions 11, 12 depicted in Figure 1 would often form source and drain contacts of such FET transistor structures.

Those skilled in the art will appreciate that the camouflaging implant 14 being a P-type implant between N-type region 11 and N-type region 12 will not provide a conducting path. The depth of the implants are controlled, as is well known in the art, by the energy used in the implanting process. Preferably, the camouflaging implant 14 is formed first and by a relatively lower energy level compared to the implant which will form the conducting channel implant 13. Implanted region 14 should have the peak of its distribution range lying close to the surface.

Thereafter, a relatively higher energy implant is performed to form region 13. The second implant, having a higher energy, should have the peak of its distribution range lying at least 2 σ distances away from the peak of the range distribution peak for implanted region 14. The value σ corresponds to the range profile distribution width for implant 14.

Due to the fact that some reverse engineers have etch and/or stain processes that can differentiate between N-type and P-type implants, the reverse engineer with such capabilities might infer the presence of the hidden conducting channel 13 by noting the presence of camouflaging region 14 if the camouflaging region 14 only occurred when it was used to hide conducting channel 13. The reverse engineer might observe region 14 (assuming the reverse engineer is able to differentiate it from regions 11 and 12 due to its different conductivity type) and, noting that it does not provide a conduction path itself, therefore conclude that region 14 has no purpose other than to hide an underlying implanted region 13. Thus, the reverse engineer might infer the presence of a conducting channel between regions 11 and 12 by the presence of the camouflaging implant 14. Thus, in order to thwart the reverse engineer with such capabilities, the relatively shallow implant 14 should be used in other places where no interconnect is desired to be formed between two adjacent active regions. See, for example, Figure 3 where there are active regions 21 and 22 associated with two different active devices. Those skilled in the art realize, of course, that when you have two adjacent active regions they may or may not be interconnected due to the particular design requirements of the circuit. In Figure 3 it is assumed that the two regions 21, 22 are not interconnected, but nevertheless a camouflaging P-type implant region 24 is formed between them. By using the structure shown in Figure 1 in some areas (where interconnects are needed) and the structure shown in Figure 3 in other areas (where interconnects are not desired), the reverse engineer will not be able to infer the presence of an interconnect by the presence of the camouflaging implant 14, 24. Of course, camouflaging implants 14 and 24 can be formed at the same time, if desired. They are given different reference numerals simply for the ease of discussion and depiction.

The configurations shown in Figures 1 and 3 will be repeated over and over again on a semiconductor chip, possibly more than a million times depending upon the complexity of the

chip. Indeed, the camouflaging implant 14, 24 may be used over essentially 100% of the area of the chip dedicated for use as interconnections and where interconnections between active regions could plausibly occur, but do not occur. As such said camouflaging implant 14, 24 preferably has a larger area, when viewed in a direction normal to a major surface of in the integrated circuit or device, than the area of the conductive channels camouflaged thereby. If the reverse engineer can not infer the presence of a conductive channel merely by the presence of the camouflaging implant 14, 24, it makes the reverse engineer have to work all that much harder to try to determine just how the active regions in an integrated circuit are interconnected. Given the fact that there can be millions of interconnections and even more places where an interconnection could exist (but does not due to the particular requirements of the circuitry on the integrated circuit chip), this invention makes it impracticable for the reverse engineer to try to work out just where the interconnection do exist.

Of course, some practicing the present invention may elect not to use a camouflaging implant 14, 24 in certain regions between two active devices, as is shown in Figure 4, to confuse matters still further for the reverse engineer. Thus, in some places, the implanted channel 13 of Figures 1 and 2 might be used without a camouflaging implant 14.

The more you confuse a reverse engineer, the more apt you are to thwart him at reverse engineering any particular integrated circuit. Therefore, other interconnection schemes can also be used in a particular IC design to camouflage further how the active regions are interconnected. Since there are millions of active regions in a large modern IC, different methods of interconnection can be combined for use together on a single IC. For example, in U.S. Patent 5,866,933 a shallow implant is used to provide an interconnection between two active regions. Thus, some practicing the present invention for some interconnects on a chip may decide to use other inventions, including the invention of our prior U.S. Patent No. 5,866,933 in order to provide other interconnections. The more you confuse the reverse engineer, the better chance you have of thwarting his efforts.

Those skilled in the art will realize that when the present invention is used in connection with the manufacture of semiconductor devices and ICs, the processes used to fabricate such ICs

and devices may require additional processing steps to use the present invention or it may be possible to utilize the present invention, by modifying the masks for making a integrated circuit, without adding additional processing steps. It basically depends upon the fabrication processes used by a manufacturer of integrated circuits. Thus, for some manufacturers, they should be able to implement the present invention without adding to the cost of manufacturing semiconductor devices and integrated circuits. For others, additional processing steps will be involved, which will add to the cost of making a semiconductor device or IC. However, the additional cost of making the device or IC may well be justified in view of the fact that the resulting device will be more robust against reverse engineering.

Figure 2 is similar to Figure 1, but the conductivity types of the various regions have been reversed. While those skilled in the art will realize, of course, that the N-type regions 11 and 12 forming the drain of a first transistor 1 and the source of a second transistor 2 is a situation which will frequently arise in an integrated circuit, the configuration of Figure 2 can occur and therefore is depicted for the sake of completeness. P-type versions of the structures shown in Figure 3 and 4 are not included herein for the sake of brevity as those P-type structures are readily apparent to those skilled in the art.

Figure 5 is a plan view of a small portion of an IC. Four FET transistors T1 - T4 are depicted together with the drains D1 - D4, sources S1 - S4 and gates G1 - G4. Drain D3 and source S4 are depicted as being interconnected by a buried implant 13-1. Drain D4 and source S2 are depicted as being interconnected by a buried implant 13-2. The regions in which interconnections could plausibly occur, but do not occur, and the regions over-lying buried interconnects 13-1 and 13-2 are all covered with a camouflaging implant 14, 24. As previously indicated, camouflaging implant 14, 24 is preferably implanted during a single implant process and is only given a different numerals herein to differentiate when it overlies an interconnect (where it is labeled by numeral 14) and when it overlies regions where interconnections could plausibly occur, but do not occur (where it is labeled by numeral 24). The regions where buried interconnection 13 occur and do not occur is governed by the particular function or functions to be performed by the IC in question. In the embodiment of Figure 5 it is clear that the

camouflaging implant 14, 24 has a significantly larger area, when viewed in a direction normal to a major surface 15 (See Figures 1 & 3) of in the IC, than the area of the conductive channels 13-1 and 13-2 camouflaged thereby.

Those skilled in the art will appreciate that the devices T1 - T4, while they are identified here as FETs in this embodiment, can represent other types of semiconductor devices with active regions some of which are interconnected by a conducting channel such as the channel 13-2 between S2 and D4 or the conducting channel 13-1 between S4 and D3. Of course, other or different interconnection patterns might well be used in practice. In any case, the conductivity type of regions 13-1, 13-2, D1, S2 and S4 (as well as the other active regions) would preferably be of a common conductivity type in this example and, for many integrated circuits, of N-type conductivity.

Having described the invention with respect to a preferred embodiment thereof, modification will now no doubt suggest itself to those skilled in the art. As such, the invention is not to be limited to the disclosed embodiments except as required by the appended claims.

What is claimed is:

1. A camouflaged interconnection scheme for interconnecting two spaced-apart implanted regions of a common conductivity type in an integrated circuit or device in a manner which inhibits reverse engineering thereof, the interconnection scheme comprising:

a first implanted region in the integrated circuit or device forming a conducting channel between the two spaced-apart implanted regions, the conducting channel being of said common conductivity type and bridging a region between said two spaced-apart regions; and

a second implanted region of opposite conductivity type in the integrated circuit or device, said second implanted region being disposed between said two spaced-apart implanted regions of common conductivity type and overlying said conducting channel.

2. The invention of claim 1 wherein said second implanted region overlying said conducting channel has a larger area, when viewed in a direction normal to a major surface of in the integrated circuit or device, than has said conducting channel.

3. The invention of claim 1 wherein said two spaced-apart implanted regions form source and/or drain contacts, respectively, of two separate field effect transistors (FETs).

4. The invention of claim 1 wherein the second implanted region is provided in said integrated circuit or device over regions having no conducting channels formed therein.

5. A camouflaged interconnection scheme for interconnecting a plurality of spaced-apart implanted regions of a common conductivity type in an integrated circuit or device, the interconnection scheme comprising:

a plurality of interconnects each interconnecting selected implant regions of said plurality of spaced-apart implanted regions, each interconnect comprising a buried conducting channel

bridging a region between the selected implant regions; and

at least one implanted region of opposite conductivity type in the integrated circuit or device, the at least one implanted region of opposite conductivity type being disposed over at least a majority of said plurality of interconnects to camouflage said at least a majority of said plurality of interconnects.

6. The invention of claim 5 wherein said at least one implanted region of opposite conductivity type has a larger area than a total area of a related at least one of said conducting channels, when viewed in a direction normal to a major surface of in the integrated circuit or device.

7. The invention of claim 5 wherein at least selected one of said spaced-apart implanted regions form source and/or drain contacts, respectively, of adjacent field effect transistors (FETs).

8. The invention of claim 5 wherein the second implanted region is provided in said integrated circuit or device over regions having no conducting channels formed therein.

9. A method of providing and camouflaging an interconnect between two adjacent implanted regions in an integrated circuit or device, the two adjacent implanted regions being of a common conductivity type, said method comprising:

implanting a first region of said common conductivity type, said first region being disposed between locations where said two adjacent implanted regions either have been or will be formed; and

implanting a second region of opposite conductivity type to said common conductivity type, said second region overlying at least said first region and having a concentration profile normal to a major surface of said integrated circuit or device with a concentration peak closer to said major surface of the semiconductor device than a concentration peak for the first implanted

region.

10. The method of claim 9, wherein said first region is implanted at a higher energy than is said second region.

11. The method of claim 9, wherein said second region is implanted before said first region is implanted.

12. The method of claim 9, wherein said first region is implanted during the implantation of active regions associated with transistors formed in said integrated circuit or device.

13. The method of claim 12 wherein said active regions are source and/or drain regions and wherein said transistors are FET devices formed in said integrated circuit or device.

14. The method of claim 9, wherein the step of implanting a second region of opposite conductivity type to said common conductivity type includes implanting said second region in regions of said integrated circuit or device where interconnections between active regions could plausibly occur but do not occur.

Abstract

A camouflaged interconnection for interconnecting two spaced-apart implanted regions of a common conductivity type in an integrated circuit or device and a method of forming same. The camouflaged interconnection comprises a first implanted region forming a conducting channel between the two spaced-apart implanted regions, the conducting channel being of the same common conductivity type and bridging a region between the two spaced-apart regions, and a second implanted region of opposite conductivity to type, the second implanted region being disposed between the two spaced-apart implanted regions of common conductivity type and over lying the conducting channel to camouflage the conducting channel from reverse engineering.

ELOS 1830140US

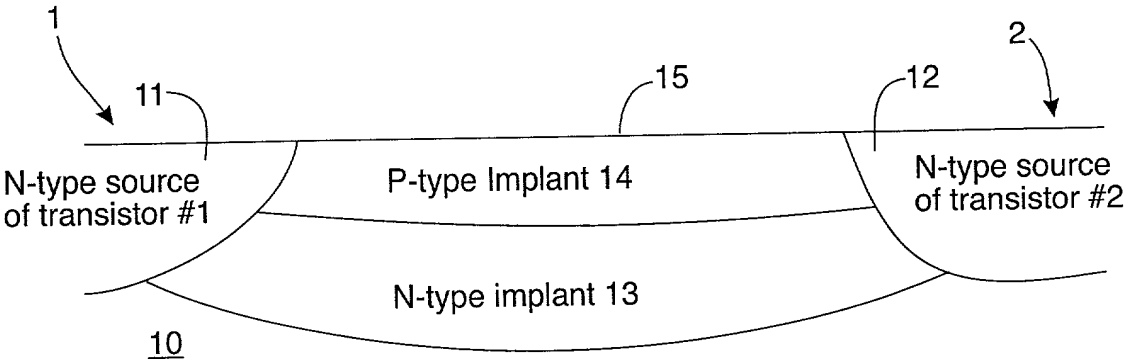

Fig. 1

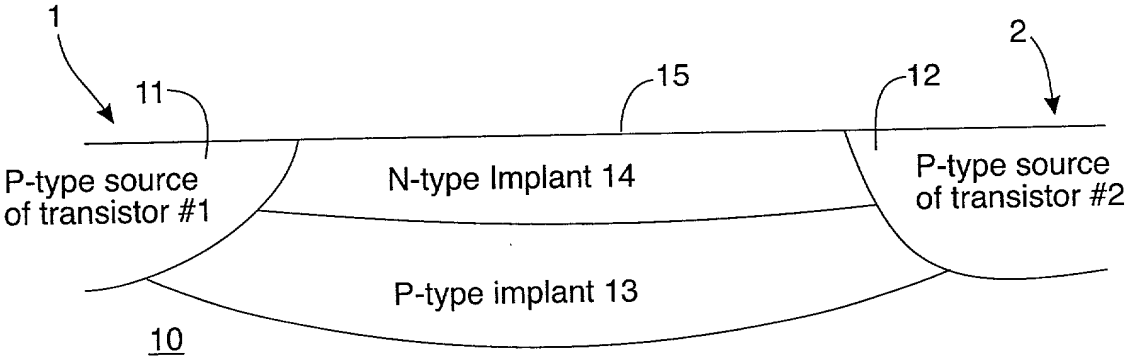

Fig. 2

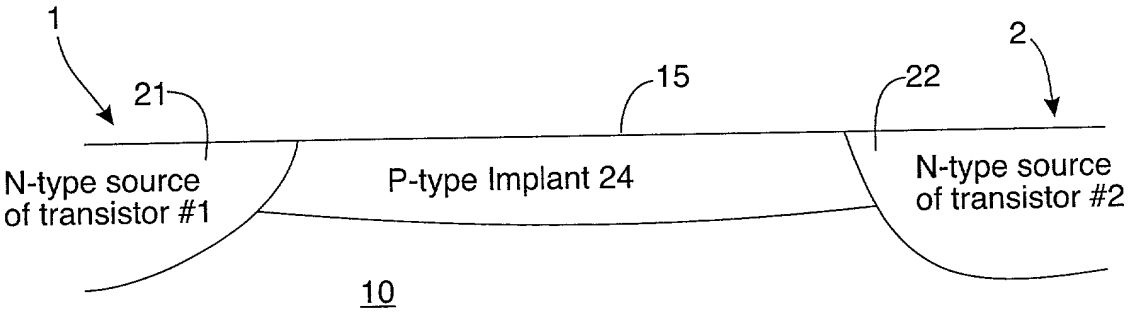

Fig. 3

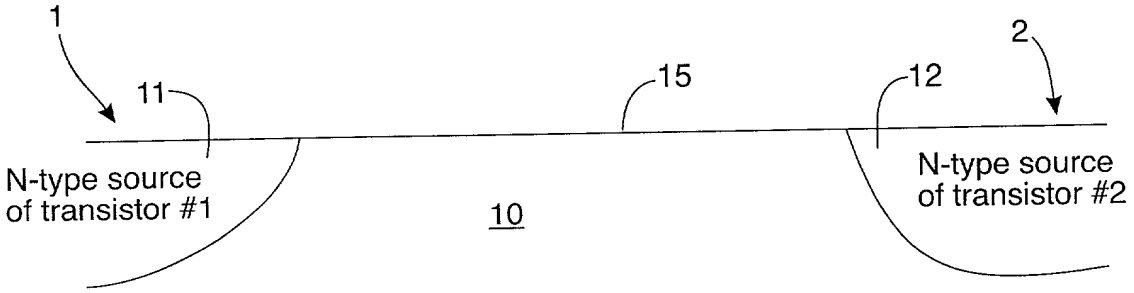

Fig. 4

prior art

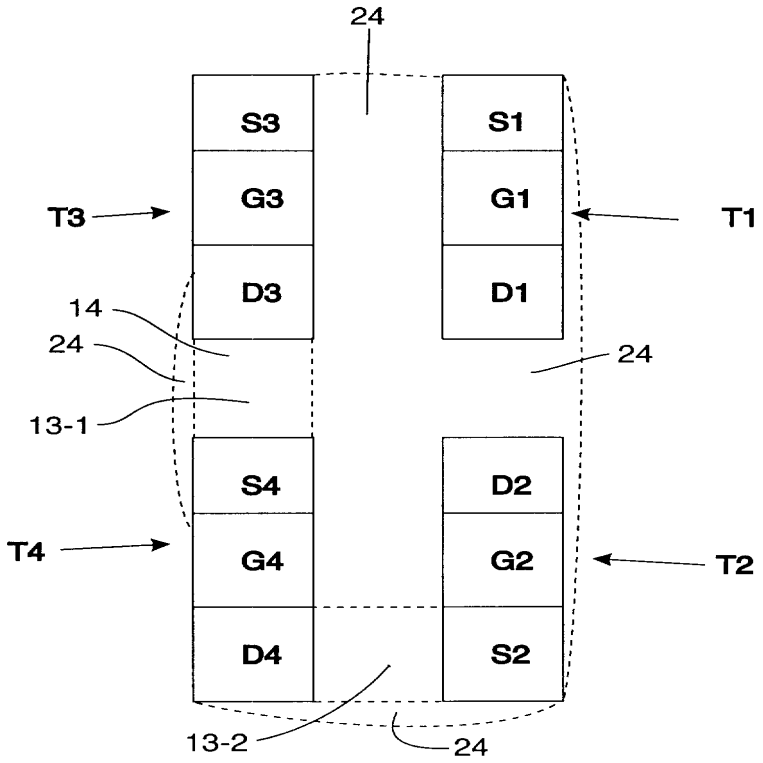

Figure 5

Attorney's Docket No. B-3650 617089-5/RPB

COMBINED DECLARATION AND POWER OF ATTORNEY

(ORIGINAL, DESIGN, NATIONAL STAGE OF PCT, SUPPLEMENTAL, DIVISIONAL, CONTINUATION, OR CIP)

As a below named inventor, I hereby declare that:

TYPE OF DECLARATION

This declaration is of the following type: *(check one applicable item below)*

[x] original
[ ] design
[ ] supplemental

NOTE: If the declaration is for an International Application being filed as a divisional, continuation or continuation-in-part application, do not check next item; check appropriate one of last three items.

[ ] national stage of PCT

NOTE: If one of the following 3 items apply, then complete and also attach ADDED PAGES FOR DIVISIONAL, CONTINUATION, OR CIP.

[ ] divisional
[ ] continuation
[ ] continuation-in-part (CIP)

INVENTORSHIP IDENTIFICATION

WARNING: If the inventors are each not the inventors of all the claims an explanation of the facts, including the ownership of all the claims at the time the last claimed invention was made, should be submitted.

My residence, post office address and citizenship are as stated below next to my name. I believe I am the original, first and sole inventor *(if only one name is listed below)* or an original, first and joint inventor *(if plural names are listed below)* of the subject matter which is claimed and for which a patent is sought on the invention entitled:

TITLE OF INVENTION

"IMPLANTED HIDDEN INTERCONNECTIONS IN A SEMICONDUCTOR DEVICE FOR PREVENTING REVERSE ENGINEERING"

SPECIFICATION IDENTIFICATION

the specification of which: *(complete (a), (b) or (c))*

(a) [X] is attached hereto.

(b) [ ] was filed on _____ as [ ] Serial No.
or [ ] Express Mail No., *as Serial No. not yet known,* _____
and was amended on _____*(if applicable).*

NOTE: Amendments filed after the original papers are deposited with the PTO which contain new matter are not accorded a filing date by being referred to in the declaration. Accordingly, the amendments involved are those filed with the application papers or, in the case of a supplemental declaration, are those amendments claiming matter not encompassed in the original statement of invention or claims. See 37 CFR 1.67.

(c) [ ] was described and claimed in PCT International Application No. _____
filed on _____ as amended under PCT Article 19 (1)
on _____ *(if any).*

ACKNOWLEDGMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code Federal Regulations § 1.56.

[ ] In compliance with this duty there is attached an information disclosure statement 37 CFR 1.97.

PRIORITY CLAIM

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign applications(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

(complete (d) or (e))

(d) [X] no such applications have been filed.
(e) [ ] such applications have been filed as follows.

NOTE: Where item (c) is entered above and the International Application which designated the U.S. claimed priority check item (e), enter the details below and make the priority claim.

EARLIEST FOREIGN APPLICATION(S), IF ANY, FILED WITHIN 12 MONTHS (6 MONTHS FOR DESIGN(S)) PRIOR TO THIS U.S. APPLICATION

COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 37 USC 119
			[ ] YES [ ] NO
			[ ] YES [ ] NO
			[ ] YES [ ] NO
			[ ] YES [ ] NO
			[ ] YES [ ] NO

ALL FOREIGN APPLICATION(S), IF ANY FILED MORE THAN 12 MONTHS (6 MONTHS FOR DESIGN(S)) PRIOR TO THIS U.S. APPLICATION

POWER OF ATTORNEY

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(List name and registration number)*

Richard P. Berg, Reg. No. 28,145
Mavis S. Gallenson, Reg. No. 32,464
Kam C. Louie, Reg. No. 33,008
Ross A. Schmitt, Reg. No. 42,529
Victor Repkin, Reg. No. 45,039
John Palmer, Reg. No. 36,885
Peter D. Galloway, Reg. No. 27, 885
William R. Evans, Reg. No. 25, 858

(check the following item, if applicable)

[ ] Attached as part of this declaration and power of attorney is the authorization of the above-named attorney(s) to accept and follow instructions from my representative(s).

SEND CORRESPONDENCE TO:

Richard P. Berg, Esq.
c/o LADAS & PARRY
5670 Wilshire Boulevard, Suite 2100
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DIRECT TELEPHONE CALLS TO:
(Name and telephone number)

Richard P. Berg

(323) 934-2300

DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

SIGNATURE(S)

Full name of **sole or first inventor** William M. Clark, Jr.
Inventor's signature X William M Clark
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Inventor's signature X James P. Baukus
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Full name of **third joint inventor**, if any Lap-Wai Chow
Inventor's signature X Lap-Wai Chow
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CHECK PROPER BOX(ES) FOR ANY OF THE FOLLOWING ADDED PAGES(S) WHICH FORM A PART OF THIS DECLARATION

[ ] Signature for third and subsequent joint inventors. *Number of pages added* _

[ ] Signature by administrator(trix), executor(trix) or legal representative for deceased or incapacitated inventor. *Number of pages added* _____

[ ] Signature for inventor who refuses to sign or cannot be reached by person authorized under 37 CFR 1.47. *Number of pages added Added* pages to combined declaration and power of attorney for divisional, continuation-in-part (CIP) application. *Number of pages added* _____

* * *

[ ] Authorization of attorney(s) to accept and follow instructions from representative.

* * *

If no further pages form a part of this Declaration then end this Declaration with this page and check the following item.

[x]This declaration ends with this page.